Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A field effect transistor (FET) comprising:
a source region;
a drain region;
a channel region disposed between the source and drain regions;
a bifurcated gate region positioned over said channel region; and
a gate oxide layer adjacent to said gate region, wherein said gate oxide layer comprises an alkali metal ion.

[c2] 2.The transistor of claim 1, further comprising:
a substrate;
an isolation layer positioned over said substrate; and
at least one fin structure disposed between the source and drain regions;
wherein said source and drain regions are positioned over said isolation layer.

[c3] 3.The transistor of claim 1, wherein said alkali metal ion comprises any of cesium and rubidium.

[c4] 4.The transistor of claim 1, wherein said transistor comprises a CMOS (complementary metal oxide semiconduc-

tor) device.

[c5] 5.The transistor of claim 4, wherein said CMOS device comprises any of a nFET configuration and a pFET configuration.

[c6] 6.The transistor of claim 5, further comprising ion implantation levels for each of said nFET configuration and said pFET configuration of approximately 3×10^{18} cm^{-3}.

[c7] 7.The transistor of claim 1, wherein said gate region comprises silicide.

[c8] 8.The transistor of claim 5, wherein said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET and pFET configurations by an amount required to match desired off-currents for said nFET and pFET configurations.

[c9] 9.A (field effect transistor) CMOS (complementary metal oxide semiconductor) device comprising:
raised source/drain regions;
a channel region disposed between said source/drain regions;
a gate region positioned over said channel region;
a silicon layer dividing said gate region; and
a gate oxide layer adjacent to said gate region, wherein

said gate oxide layer comprises an alkali metal ion.

[c10] 10. The device of claim 9, further comprising:
a substrate;
an isolation layer positioned over said substrate; and
at least one fin structure disposed between the source and drain regions;
wherein said source/drain regions are positioned over said isolation layer.

[c11] 11.The device of claim 9, wherein said alkali metal ion comprises any of cesium and rubidium.

[c12] 12.The device of claim 9, further comprising any of a nFET region and a pFET region.

[c13] 13.The device of claim 12, comprising ion implantation levels for each of said nFET region and pFET region of approximately 3×10^{18} cm^{-3}.

[c14] 14.The device of claim 9, further comprising spacers separating said gate region from said source/drain regions.

[c15] 15.The device of claim 9, wherein said gate region comprises silicide.

[c16] 16.The device of claim 12, wherein said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET

and pFET regions by an amount required to match desired off-currents for said nFET and pFET regions.

[c17] 17.A method of tuning a threshold voltage of nFET (field effect transistor) and pFET devices in a double-gate CMOS (complementary metal oxide semiconductor) integrated circuit structure, said method comprising:
performing a PSP (post silicide probe) electrical test on said double-gate CMOS integrated circuit structure;
determining nFET and pFET threshold voltages during said PSP electrical test; and
implanting said double-gate CMOS integrated circuit structure with an alkali metal ion.

[c18] 18.The method of claim 17, wherein said implanting adjusts said nFET and pFET threshold voltages by an amount required to match desired off-currents for said nFET and pFET devices.

[c19] 19.The method of claim 17, wherein prior to said performing, said method comprises:
forming a fin structure on a substrate;
forming source/drain regions over said fin structure;
forming a channel region between said source/drain regions;
depositing a gate oxide layer adjacent to said source/drain regions; and

forming a gate region over said gate oxide layer and said fin structure.

[c20] 20. The method of claim 19, further comprising forming an isolation layer on said substrate.

[c21] 21.The method of claim 17, wherein said alkali metal ion comprises any of cesium and rubidium.

[c22] 22.The method of claim 17, wherein ion implantation levels for said nFET and pFET devices are determined during said PSP test.

[c23] 23.The method of claim 17, wherein ion implantation levels for each of said nFET and pFET devices is approximately 3×10^{18} cm^{-3}.